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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,299	06/07/2001	Sanjay Ramakrishna Pillay	1081-CA	9525

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EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2115	3

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,299	PILLAY ET AL.	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,7-11,14-18 and 20* is/are rejected.

7)☒ Claim(s) *2-4,6,12,13 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been presented for examination.

Claim Objections

2. Claim 8 is objected to because of the following informalities: It is claimed that a *lower* speed clock is selected in order to *increase* an operating frequency. In order to *increase* operating frequency a *high* speed clock would have to be selected and for examining purposes the claim has been interpreted as such. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 9-11, 16-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins et al [Jenkins] US Pat No 6668318 in view of Watts, Jr et al [Watts] US Pat No 6633988.

5. Referring to claim 1, Jenkins teaches the invention substantially including:

a. reducing the processing clock to increase the duty cycle of the processing engine.

In summary, Jenkins teaches operating the processing engine at a minimum processing speed by reducing the speed of the processing engine [col. 1 lines 49-51 and col. 2 lines 30-38]. Reducing the processing speed inherently increases the duty cycle of the processing engine since it takes longer to process data. Although Jenkins teaches monitoring the demands on the processing engine, Jenkins does not explicitly teach estimating the duty cycle of the processing

engine. In addition, Jenkins also does not explicitly teach generating a plurality of lower speed clocks from a high speed clock and that one of the generated lower speed clocks are used to increase the duty cycle of the processing engine.

Watts explicitly teaches, monitoring the processing engine by calculating its duty cycle in order to reduce processor idle time [Abstract, col. 6 lines 3-5 and col. 12 line 61-col. 13 line 5]. Calculating T(on) vs. T(off) is the same as calculating the duty cycle. It would have been obvious to include the duty cycle calculating means taught in Watts into the Jenkins system because Watts teaches that it will help reduce the amount of idle time experienced by the processing engine which inherently increases the duty cycle of the processing engine.

There are many different methods known in the art to generate lower speed clocks including dividing a high speed clock into lower speed clocks. It is obvious that this method could be used in the Jenkins-Watts system and that the lower speed clocks could be gated (i.e. selected) in order to reduce the processing speed of the processing engine.

6. Referring to claim 5, the Transmeta processor taught by Jenkins is interpreted as a digital signal processor.

7. Referring to claim 9, this is rejected on the same basis as set forth hereinabove. Jenkins and Watts teach the system and therefore teach the method performed by the system.

In particular, processor loading is interpreted as the processor being active as opposed to being inactive and thus inherently affects the duty cycle of the processor. Because of this, it is further interpreted that calculating the duty cycle of the processor inherently estimates processor loading. Furthermore, the Jenkins-Watts system teaches that operating frequency is adjusted

based on the determination of the calculated duty cycle in order to operate at a minimal speed, which would inherently distribute processor loading across a particular block of time.

8. Referring to claim 10, Watts teaches calculating the time a processor is active vs. a time the processor is inactive thus determining the duty cycle of the processor within a period of time [col. 6 lines 3-5]. Although Watts does not explicitly teach how the times are calculated it is obvious that the times could be calculated by counting a number of clock periods.

9. Referring to claim 11, this is rejected on the same basis as set forth hereinabove. Jenkins and Watts teach the system and therefore teach the method performed by the system.

10. Referring to claim 16, 18 and 20, these are rejected on the same basis as set forth hereinabove. It is well known that computer processors can process blocks of audio data.

11. Referring to claim 17, multiprocessors composed on a single chip are well known in the art. It is obvious that the Jenkins-Watts system could be applied to those chips as well.

12. Claims 7-8 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins and Watts as applied to claim 1, 5, 9-11, 16-18 and 20 above, and further in view of Felts, III et al [Felts] US Pat No 6581164.

13. Referring to claims 7 and 8, the Jenkins-Watts system does not explicitly teach detecting underflow conditions in a buffer and selecting a high or low speed clock to increase the operating frequency of the processing engine in result of the underflow detection. In summary, the Jenkins-Watts system does not teach having the processor output data to a buffer faster to overcome the underflow condition. Felts teaches monitoring a buffer and determining the buffers "fullness" in order to adjust clock frequencies [col. 15 lines 28-39]. It would have been

obvious to one of ordinary skill in the art to modify the Jenkins-Watts to increase the operating frequency supplied to the processing engine when an underflow is detected because it would ensure that the processing engine would not operate too slowly but still maintain "the minimum processing speed required to robustly run" [Jenkins col. 1 lines 49-52].

14. Referring to claim 14, this is rejected on the same basis as set forth hereinabove. Jenkins, Watts and Felts teach the system and therefore teach the method performed by the system.

15. Referring to claim 15, Felts teaching monitoring a dipstick [fig. 11].

Allowable Subject Matter

16. Claims 2-4, 6, 12-13 and 19 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (703) 305-7849. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark Connolly
Examiner
Art Unit 2115

mc
July 23, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100